**Listing of Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled).

2. (Withdrawn) The method according to claim 1, further comprising:

multiplying the sum with an inverse of the check vector to find the next free bit.

3. (Withdrawn) An apparatus for performing the method according to claim 1, the apparatus comprising:

a calculator for obtaining the value P of the current pointer;

a generator for generating the add vector; and

an adder for adding the add vector to the check vector.

4. (Withdrawn) The apparatus according to claim 3, further comprising:

a multiplier for multiplying the sum with an inverse of the check vector to find the next free bit.

5. (Withdrawn) An apparatus for performing the method according to claim 1, the apparatus comprising:

means for obtaining the value P of the current pointer;

means for generating the add vector; and

means for adding the add vector to the check vector.

6. (Withdrawn) The apparatus according to claim 5, further comprising:

means for multiplying the sum with an inverse of the check vector to find the next free bit.

7. (Cancelled).

8. (Withdrawn) The method according to claim 7, wherein the available part is a part pointed to by the current pointer.

9. (Withdrawn) The method according to claim 8, further comprising:

finding a free bit in the available part.

10. (Withdrawn) The method according to claim 9, wherein the step for finding a free bit comprises:

breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein $0 \leq U \leq 2^{Y}-1$, and $0 \leq L \leq 2^{X-Y}-1$, where all of X, Y, U, and L are integers;

obtaining an add vector by setting its bit number L;

adding the add vector to the available part to obtain a sum; and

multiplying the sum with an inverse of the available part.

11. (Cancelled).

12. (Currently Amended) ~~The method according to claim 11,~~ A method for finding a next empty bit in a register having N bits and a current pointer pointing to one of the bits, the method comprising:

breaking the N bits of a check vector in the register into M parts, wherein N and M are integers and 1< M<N; and

selecting an available part that has an empty bit;

wherein the available part is a first part, having an empty bit, to the left of the part pointed to by the current pointer; and

wherein the step for selecting the available part comprises:

breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein $0 \leq U \leq 2^{Y}-1$, and $0 \leq L \leq 2^{X-Y}-1$, where all of X, Y, U, and L are integers;

creating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts;

obtaining an add vector by setting its bit number U;

adding the add vector to the check sector to obtain a sum; and

multiplying the sum with an inverse of the check sector.

13. (Cancelled).

14. (Currently Amended) ~~The method according to claim 13,~~ A method for finding a next empty bit in a register having N bits and a current pointer pointing to one of the bits, the method comprising:

breaking the N bits of a check vector in the register into M parts, wherein N and M are integers and 1< M<N; and

selecting an available part that has an empty bit;

wherein the available part is a first part, having an empty bit, to the left of the part pointed to by the current pointer;

the method further comprising finding an empty bit in the available part; and

wherein the step for finding an empty bit comprises:

increasing the available part by 1; and

multiplying the increased available part with an inverse of the available part.

15. (Withdrawn) The method according to claim 7, wherein the available part is a first part, having a free bit, from the beginning of the register.

16. (Withdrawn) The method according to claim 15, wherein the step for selecting the available part comprises:

creating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts;

increasing the check sector by 1; and

multiplying the increased check sector with an inverse of the check sector.

17. (Withdrawn) The method according to claim 15, further comprising finding a free bit in the available part.

18. (Withdrawn) The method according to claim 17, wherein the step for finding a free bit comprises:

increasing the available part by 1; and

multiplying the increased available part with an inverse of the available part.

19. (Currently Amended) ~~The method according to claim 7, further~~ A method for finding a next empty bit in a register having N bits and a current pointer pointing to one of the bits, the method comprising:

breaking the N bits of a check vector in the register into M parts, wherein N and M are integers and 1< M<N;

selecting an available part that has an empty bit;

creating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts; and

deciding whether the register has a free bit by performing an AND operation to all bits of the check sector.

20. (Cancelled).

21. (Withdrawn) The apparatus according to claim 20, wherein the selector selects a part pointed to by the current pointer as the available part.

22. (Cancelled).

23. (Cancelled).

24. (Cancelled).

25. (Currently Amended) ~~The apparatus according to claim 24,~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

a first breaker for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and $1< M<N$; and

a selector for selecting an available part that has an empty bit, wherein the selector selects the available part on the left of the part pointed to by the current pointer;

a first breaker for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and $1< M<N$; and

a check sector generator for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts; and

a second breaker for breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein $0\leq U\leq 2^{Y}-1$, and $0\leq L\leq 2^{X-Y}-1$, where all of X, Y, U, and L are integers;

wherein the selector comprises:

an add vector generator, setting bit number U of the add vector;

an adder for adding the add vector to the check sector to obtain a sum; and

a multiplier for multiplying the sum with an inverse of the check sector.

26. (Withdrawn) The apparatus according to claim 20, wherein the selector selects the available part from the beginning of the register.

27. (Withdrawn) The apparatus according to claim 26, further comprising:

a check sector generator for generating a check sector, wherein each bit of the check

sector results from performing an AND operation to all bits of a corresponding part of the M parts.

28. (Withdrawn) The apparatus according to claim 27, wherein the selector comprises:

an adder for increasing the check sector by 1; and

a multiplier for multiplying the increased check sector with an inverse of the check sector.

29. (Cancelled).

30. (Cancelled).

31. (Cancelled).

32. (Currently Amended) ~~The apparatus according to claim 31,~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

a first breaker for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and $1< M<N$;

a selector for selecting an available part that has an empty bit;

a second breaker for breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein $0\leq U\leq 2^{Y}-1$, and $0\leq L\leq 2^{X-Y}-1$, where all of X, Y, U, and L are integers; and

an empty bit finder, wherein the empty bit finder finds an empty bit on the left of the bit pointed to by the current pointer;

wherein the empty bit finder comprises:

an add vector generator, setting bit number L of the add vector;

an adder for adding the add vector to the available part to obtain a sum; and

a multiplier for multiplying the sum with an inverse of the available part.

33. (Cancelled).

34. (Currently Amended) ~~The apparatus according to claim 33,~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

a first breaker for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and $1< M<N$;

a selector for selecting an available part that has an empty bit; and

an empty bit finder, wherein the empty bit finder finds an empty bit from the beginning of the available part;

wherein the empty bit finder comprises:

an adder for increasing the available part by 1; and

a multiplier for multiplying the increased available part with an inverse of the available part.

35. (Currently Amended) ~~The apparatus according to claim 20, further comprising:~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

a first breaker for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and 1< M<N;

a selector for selecting an available part that has an empty bit;

a check sector generator for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts; and

a register status unit for performing an AND operation to all bits of the check sector.

36. (Currently Amended) The apparatus according to claim **[[**20**]]** 35, further comprising:

a next vector generator for generating the next vector with the found empty bit masked.

37. (Cancelled).

38. (Withdrawn) The apparatus according to claim 37, wherein the selecting means selects the part pointed to by the current pointer as the available part.

39. (Currently Amended) The apparatus according to claim **[[**37**]]** 49, wherein the selecting means selects the available part on the left of the part pointed to by the current pointer.

40. (Currently Amended) The apparatus according to claim **[[**39**]]** 51, further comprising:

means for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts.

41. (Withdrawn) The apparatus according to claim 40, further comprising:

means for breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein $0 \leq U \leq 2^{Y}-1$, and $0 \leq L \leq 2^{X-Y}-1$, where all of X, Y, U, and L are integers.

42. (Withdrawn) The apparatus according to claim 41, wherein the selecting means comprises:

means for generating an add vector, setting bit number U of the add vector;

means for adding the add vector to the check sector to obtain a sum; and

means for multiplying the sum with an inverse of the check sector.

43. (Withdrawn) The apparatus according to claim 37, wherein the selecting means selects the available part from the beginning of the register.

44. (Withdrawn) The apparatus according to claim 43, further comprising:

means for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts.

45. (Withdrawn) The apparatus according to claim 44, wherein the selecting means comprising:

means for increasing the check sector by 1; and

means for multiplying the increased check sector with an inverse of the check sector.

46. (Cancelled).

47. (Cancelled).

48. (Cancelled).

49. (Currently Amended) ~~The apparatus according to claim 48,~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

means for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and $1< M<N$; and

means for selecting an available part that has an empty bit;

a second means for breaking the current pointer into upper bits and lower bits, wherein the current pointer has X bits, the upper bits have Y bits and a value U, and the lower bits have X-Y bits and a value L, and wherein $0 \leq U \leq 2^{Y}-1$, and $0 \leq L \leq 2^{X-Y}-1$, where all of X, Y, U, and L are integers; and

means for finding the empty bit, wherein the empty bit finding means finds the empty bit on the left of the bit pointed to by the current pointer;

wherein the empty bit finding means comprises:

means for generating an add vector, setting bit number L of the add vector;

means for adding the add vector to the available part to obtain a sum; and

means for multiplying the sum with an inverse of the available part.

50. (Cancelled).

51. (Currently Amended) ~~The apparatus according to claim 50,~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

means for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and 1< M<N; and

means for selecting an available part that has an empty bit; and

means for finding the empty bit, wherein the empty bit finding means finds the empty bit from the beginning of the available part;

wherein the empty bit finding means comprises:

means for increasing the available part by 1; and

means for multiplying the increased available part with an inverse of the available part.

52. (Currently Amended) ~~The apparatus according to claim 37, further~~ An apparatus for finding a next free empty bit in a register having N bits and a current pointer pointing to one of the bits, the apparatus comprising:

means for breaking the N bits of the check vector in the register into M parts, wherein N and M are integers and 1< M<N;

means for selecting an available part that has an empty bit;

means for generating a check sector, wherein each bit of the check sector results from performing an AND operation to all bits of a corresponding part of the M parts; and

means for performing an AND operation to all bits of the check sector.

53. (Currently Amended) The apparatus according to claim 37, further comprising:

means for generating the next vector with the found **[[**free**]]** empty bit masked.

54. (Withdrawn) A buffer management system comprising the apparatus according to claim 20, wherein the system allocates buffers to the register.

55. (Withdrawn) The buffer management system according to claim 54, further comprising:

an allocation state machine for controlling the apparatus; and

an allocation memory for providing a new line to the register.

56. (Withdrawn) The buffer management system according to claim 55, further comprising a buffer management state machine for controlling buffer allocation to the register.

57. (Withdrawn) The buffer management system according to claim 55, further comprising a clear arbiter for clearing the buffers allocated to the register.

58. (Withdrawn) The buffer management system according to claim 55, further comprising an allocation arbiter for arbitrating between at least two requests for buffers.

59. (Withdrawn) The buffer management system according to claim 55, further comprising an allocation counter for counting the allocated buffers.

60. (Withdrawn) The buffer management system according to claim 55, further comprising a reclaim mechanism.

61. (Withdrawn) A buffer management system comprising the apparatus according to claim 37, wherein the system allocates buffers to the register.

62. (Withdrawn) The buffer management system according to claim 61, further comprising:

means for controlling the apparatus; and

means for providing a new line to the register.

63. (Withdrawn) The buffer management system according to claim 62, further comprising means for controlling buffer allocation to the register.

64. (Withdrawn) The buffer management system according to claim 62, further comprising means for clearing the buffers allocated to the register.

65. (Withdrawn) The buffer management system according to claim 62, further comprising means for arbitrating between at least two requests for buffers.

66. (Withdrawn) The buffer management system according to claim 62, further comprising means for counting the allocated buffers.

67. (Withdrawn) The buffer management system according to claim 62, further comprising means for reclaiming buffers.

68. (Withdrawn) A computer software product containing program code for performing the method according to claim 1.

69. (Withdrawn) A computer software product containing program code for performing the method according to claim 2.

70. (Cancelled).

71. (Withdrawn) A computer software product containing program code for performing the method according to claim 8.

72. (Withdrawn) A computer software product containing program code for performing the method according to claim 9.

73. (Withdrawn) A computer software product containing program code for performing the method according to claim 10.

74. (Cancelled).

75. (Cancelled).

76. (Cancelled).

77. (Cancelled).

78. (Withdrawn) A computer software product containing program code for performing the method according to claim 15.

79. (Withdrawn) A computer software product containing program code for performing the method according to claim 16.

80. (Withdrawn) A computer software product containing program code for performing the method according to claim 17.

81. (Withdrawn) A computer software product containing program code for performing the method according to claim 18.

82. (Cancelled).

83. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 54.

84. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 55.

85. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 56.

86. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 57.

87. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 58.

88. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 59.

89. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 60.

90. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 61.

91. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 62.

92. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 63.

93. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 64.

94. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 65.

95. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 66.

96. (Withdrawn) A switching device for controlling communication of signals between a source and an output, wherein the switching device comprises the buffer management system of claim 67.